ALU-based low-power architecture is based on clock gating and a carry select adder.

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ABSTRACT:

The central processing units (CPUs) found in desktops, laptops, and other general-purpose personal computers use several watts of electricity due to their increased complexity and speed. Computer processing units aren't complete without the ALU. It carries out operations that are mathematical and logical in nature. As the complexity of the processes within the CPU grows, the ALU gets more intricate, expensive, space-consuming, and power-draining. Because of this, designing CPUs with the ALU's power consumption in mind is essential. This research recommends constructing an ALU utilizing latch free clock gating, which entails turning off unused parts of the design while concentrating on one area, to get minimal power usage. When a carry select adder (CSLA) is used as the primary computing element of the arithmetic unit, it is expected to further enhance efficiency for speedy arithmetic operations. It is clear from the CSLA's design that there is potential to reduce its environmental impact and energy consumption. To significantly reduce the CSLA's footprint and energy usage, this research employs a simple and efficient gate-level modification. We used this adjustment as a starting point for our 16-bit square root CSLA (SQRT CSLA) design, which we then compared to the original. Although it consumes less power and space than the traditional SQRT CSLA, the proposed architecture has a somewhat longer latency. A low-power 16-bit ALU for the Xilinx Spartan 3EFPGA is designed and implemented in HDL in this study.

KEYWORDS :

Concepts such as ALU, clock power, clock gating, low power, FPGA, HDL programming, and carry select adder (CSLA) are included.

INTRODUCTION

As technology advances, the number of transistors needed for any particular digital logic design is growing at an exponential rate.One major factor influencing power consumption is the number of transistors in a device, as this directly correlates to the amount of heat it generates [1]. Because most portable electronics run on batteries, reducing power consumption extends the life of the batteries, improves performance and reliability, and lowers the cost of heat removal—all of which are more significant in the modern day. Because of this, optimizing the design to decrease power consumption and increase the device's speed is always an important goal. The ideal layout allows for optimum throughput with little power consumption and a tiny footprint. However, there are situations when area, speed, and strength are incompatible; so, a balance between them is necessary. Power optimization is a possibility across the whole digital design cycle, even though the benefits are most noticeable at the architectural and algorithmic design levels. Modern microprocessors are designed to meet performance requirements with a minimum of size, power consumption, and maximum speed. Often called an ALU, this digital electrical circuit can perform arithmetic and bitwise logical operations on integer binary numbers. The ALU, a fundamental component of all computationally demanding units such as the CPU, FPU, and GPU, is often constantly involved in the data flow when an instruction decoder is being performed. To meet these demands, an ALU with good performance and minimal power consumption is needed. This necessitates keeping the ALU's power consumption low.

Exploration of Power and Where It Comes From

Processing unit power consumption is affected by a number of factors, including dynamic power consumption, power consumption in a short circuit, and power loss due to leakage currents in transistors.

PCPU = Pym + PS + Plea

The two primary categories into which these abilities fall are:

A low-power ALU architecture cannot be complete without an efficient adder for the propagation and generation block. The current bit position total cannot be generated by the elementary adder until the previous bit position sum is established and a carry is transferred into the next position. One of the fastest adders available, the Carry Select Adder

(CSLA) is used by many data-processing processors. A lot of computer systems use the CSLA to get around the problem of carry propagation delay; it does this by generating a bunch of carriers individually and then picking one to add up. Due to the usage of several sets of Ripple Carry Adders (RCA) to generate partial sum and carry, which takes into consideration carry input can = 0 and can = 1, and multiplexers (mux) to choose the final sum and carry, the CSLA shown in Figure 4 is not space efficient. The regular structure of the CSLA makes it easy to see where energy consumption and environmental impact might be reduced. To significantly reduce the CSLA's footprint and energy usage, this research employs a simple and efficient gate-level modification. While there is a little increase in latency, the proposed configuration consumes less energy and utilizes less space than traditional CSLAs. Figure 5 shows a possible design for a smaller and less power-hungry conventional CSLA that uses a Binary to Excess-1 Converter (BEC) instead of the RCA with can = 1 that is often utilized in such a design [6], [7]. One major benefit of this BEC logic is that it uses less logic gates compared to RCA's n-bit Full Adder (FA) design.

Clock gating techniques may be optimized for use in very large scale integration (VLSI) circuits in a variety of ways. They may be either: • Codesigns that do not use latches • Codesigns that do use latches.

Choose your aisle carefully since it takes up little room and uses less power.

For an ALU's propagation and generation block to be designed with minimal power consumption in mind, a very efficient adder is essential. After forming the sum of the bits in the previous position and communicating a carry into the place after it, the elementary adder will only create the total for the current bit location. In many data processing processors, you may find the Carry Select Adder (CSLA), which is known as one of the rapid adders. With the use of the CSLA, several computers may circumvent the carry propagation delay issue by constructing numerous carriers separately and then adding them together. Figure 4 shows a space-inefficient CSLA that uses several sets of Ripple Carry Adders (RCA) to create partial sums and carries while taking can = 0 and can = 1 into consideration throughout the calculation. (a mixture). Numerous energy and material efficiency modifications may be easily implemented into the CSLA because of its modular design. This study suggests a simple way to lower the CSLA's power consumption and negative effects on the environment by simply changing the gate height. The suggested layout requires less space and energy than conventional CSLAs while just marginally increasing delay. Although the RCA with can = 1 is often used in CSLAs, a Binary to Excess-1 Converter may be utilized in its place to decrease system size and power consumption, as seen in Figure 5 [6, 7]. (BEC). The main advantage of this BEC logic over the RCA's n-bit Full Adder (FA) design is the reduced number of logic gates that are required.

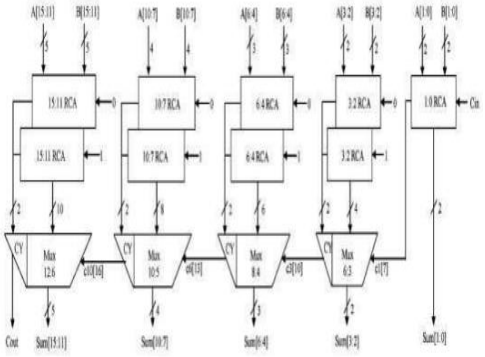

Figure 1 Regular structure of carry select adder'

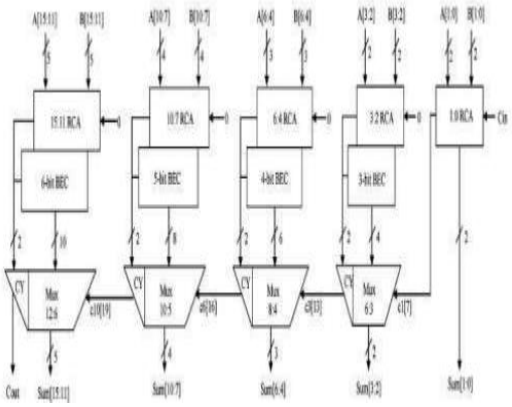

Figure 2 Proposed structure of carry select undervalue

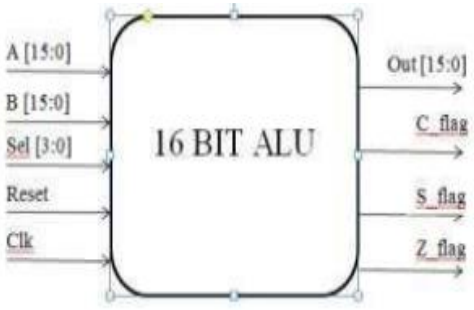

Figure 3Conventional ALU.

To evaluate the proposed ALU's efficacy in comparison to the conventional ALU shown in Figure 8, we provide the latter. The ALU requires five different inputs. There are a few other keys you may utilize besides sale, reset, and calk: A and B. You will get the result of the ALU computation in the out variable after it is finished. The ALU accepts two 16-bit values, A and B, as input. After the instruction decoder retrieves an opcode, the input

sell [3:0] selects the correct ALU operation. The reset input parameter is crucial to the process.

RESULTS

We first provide the results of our simulations and implementations, then the experimental data for both the proposed and existing models. See the RTL schematic and timing waveform of an ALU without clock gating in Figures 10 and 11. Figure 12 shows the time waveform of the adder utilized in the proposed model, whereas Figure 13 shows the RTL schematic of the same device. Figure 14 shows the timing waveform of an ALU with clock gating, whereas Figure 15 shows the RTL architecture of the same unit.

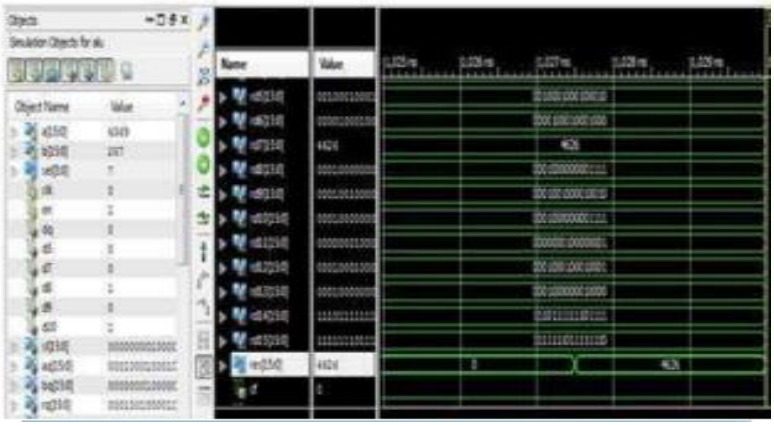

Figure 4 Simulated waveform of conventional model.

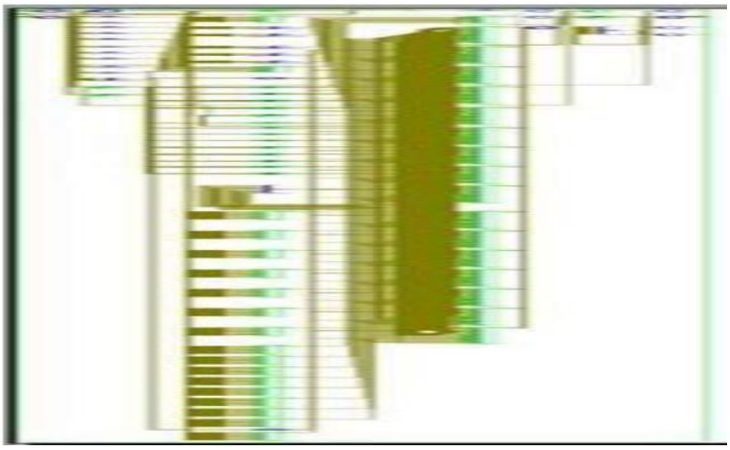

Figure 5 RTL schematic of conventional model.

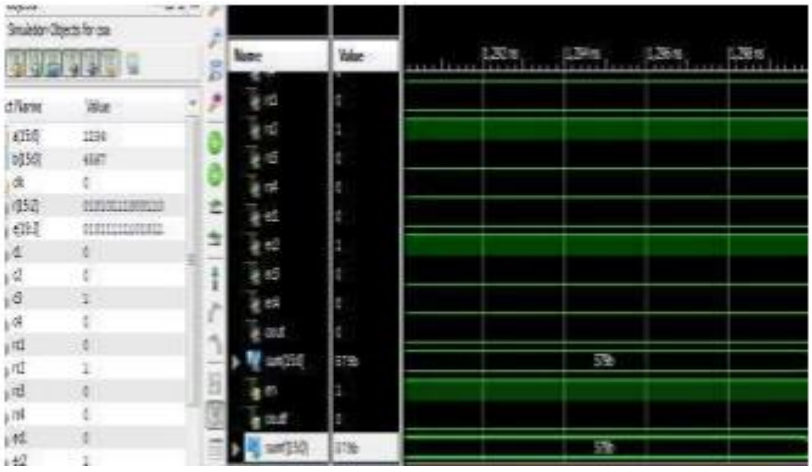

Figure 6 Simulated waveform of CSLA.

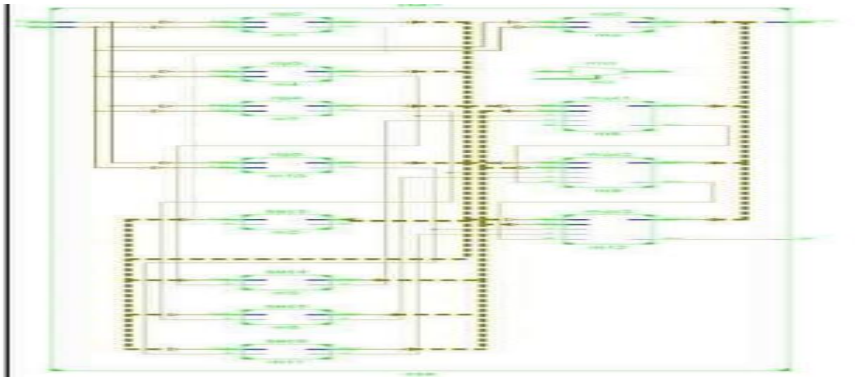

Figure 7 RTL schematic of CSLA.

Figure 8 Simulated waveform of proposed model.

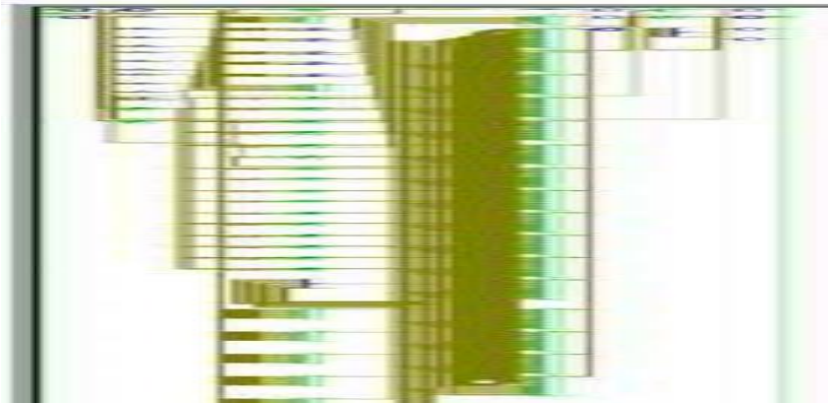

Figure 9 RTL Schematic of proposed model

Table 1Device utilization summery of conventional model

Device Utilization Summary (estimated values)			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	288	4656	6%
Number of Slice Flip Flops	150	9312	1%
Number of 4 input LUTs	518	9312	5%
Number of bonded IOBs	57	232	24%
Number of GCLKs	1	24	4%

Table 2 Device utilization summery of proposed model

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	387	4656	8%
Number of Slice Flip Flops	181	9312	1%
Number of 4 input LUTs	686	9312	7%
Number of bonded IOBs	57	232	24%
Number of GCLKs	1	24	4%

Table 1 and 2 shows the implementation results of both the models using SPARTAN 3E FPGA, realizes that clock gating technique adds the extra hardware to circuit and reduction in power is shown with table 4.it is formulated as

Table 3 Power comparison of both models

Parameter	Conventional model (mW)	Proposed model (mW)
Total power	209	198
Dynamic power	130	119
Quiescent power	79	79

CONCLUSION

We used an XILINX SPARTAN 3E FPGA to implement the previously described models after they had been designed in VERILOG and simulated in the XILINX ISE 12.1 design suite. We then compared the output to the original models. The results show that a clock-gated 16-bit ALU consumes less power than a conventional ALU. Clock gating is a powerful tool in the proposed architecture for reducing dynamic and clock power consumption by limiting the number of times an idle module's data and clock buses are switched on and off while the active module is processing. Power optimization has progressed from its original focus on the synthesis, placement, and routing stages to include the system level and RTL stages.

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